PPLN-Based Flexible Optical Logic AND Gate

Jian Wang, Junqiang Sun, Qizhen Sun, Dalin Wang, Xinliang Zhang, Dexiu Huang, and M. M. Fejer

***Abstract*—All-optical flexible 20-Gb/s logic AND gate based on cascaded sum- and difference-frequency generation in a periodically poled lithium niobate waveguide is proposed and experimentally demonstrated. The theoretical analyses further indicate that 40-, 80-, and 160-Gb/s ultrahigh-speed logic AND operations can potentially be performed. Moreover, it is expected that the AND output can be tuned in a wide wavelength range (~67 nm) with slight fluctuation of the Q-factor and extinction ratio.**

***Index Terms*—All-optical logic gate, cascaded sum- and difference-frequency generation (cSFG/DFG), optical signal processing, periodically poled lithium niobate (PPLN).**

I. Introduction

ALL-OPTICAL logic gates have attracted considerable interest in optical signal processing systems. As one of the basic and important logic functions, the all-optical logic AND gate has seen potential applications in optical switching and optical half-adder. Previously, the all-optical logic AND gate based on cascaded semiconductor optical amplifiers [1] has been proposed and demonstrated, showing impressive operation performance. Recently, with the increased research on a new promising candidate for all-optical signal processing called periodically poled lithium niobate (PPLN) waveguide [2]–[7], PPLN-based all-optical logic AND gates have been also presented [8]–[11]. In addition to complete transparency and no excess noise, ultrafast response is also attractive property of PPLN. However, the reported PPLN-based logic AND gates were short of tunability for fixed input data signals [8] or operated at the continuous-wave (CW) situation [9] or relatively low speed (5 Gb/s) [8], [11]. We have previously demonstrated 20-Gb/s logic AND gate with dual-channel AND outputs [10]. Nevertheless, such function requires two data signals set close to each other and fixed CW control, and therefore, results in the deficiency lacking of flexibility.

In this letter, we propose a simple realization of a flexible all-optical logic AND gate based on cascaded sum- and difference-frequency generation (cSFG/DFG) in a PPLN waveguide. Two approaches for 20-Gb/s logic AND operations are demonstrated in the experiment. Furthermore, the feasibility of ultrahigh-speed logic AND gates at 40, 80, and 160 Gb/s as well as the tunable performance are also investigated and theoretically analyzed in detail.

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J. Wang, J. Sun, Q. Sun, D. Wang, X. Zhang, and D. Huang are with the Wuhan National Laboratory for Optoelectronics, School of Optoelectronic Science and Engineering, Huazhong University of Science and Technology, Wuhan, 430074 Hubei, China (e-mail: jqsun@mail.hust.edu.cn).

M. M. Fejer is with the Edward L. Ginzton Laboratory, Stanford University, Stanford, CA 94305 USA.

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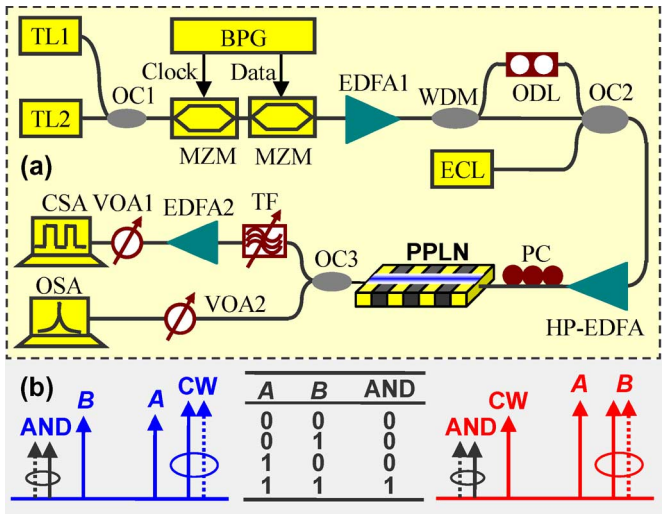

Fig. 1. (a) Experimental setup and (b) operation principle for the PPLN-based logic AND gate. TF: tunable filter. VOA: variable optical attenuator.

II. Experimental Setup and Operation Principle

Fig. 1 shows the experimental setup and operation principle for a PPLN-based logic AND gate. Two tunable lasers (TLs) and two cascaded Mach–Zehnder modulators (MZMs) driven by a bit pattern generator (BPG) are used to produce two pseudorandom binary sequence (PRBS) return-to-zero (RZ) signals (A, B) at 20 Gb/s. After passing through an erbium-doped fiber amplifier (EDFA), two data signals are separated by a wavelength-division multiplexer (WDM) with one signal delayed integral bit period relative to the other by an optical delay line (ODL). The CW control generated from an external cavity laser (ECL), together with two data signals, are combined by an optical coupler (OC), amplified by a high-power EDFA (HP-EDFA) with a small-signal gain of 40 dB and a saturation output power of 30 dBm, adjusted by a polarization controller (PC), and finally fed into PPLN to participate in the cSFG/DFG nonlinear interactions. A 50-mm-long PPLN waveguide fabricated by the electric-field poling method and annealing proton-exchanged technique is used in the experiment. It has a microdomain period of 14.7 μm and a quasi-phase matching (QPM) wavelength of 1543.2 nm at room temperature. The optical spectra are monitored by an optical spectrum analyzer [(OSA) Anritsu MS9710C], and the temporal waveforms are observed through a communications signal analyzer [(CSA) Tektronix 8000B].

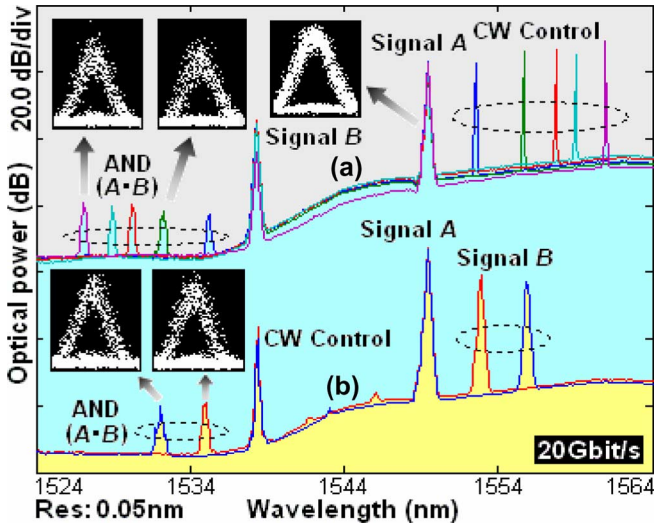

Fig. 2. Optical spectra for the 20-Gb/s logic AND gate. (a) Tunable AND output under different CW control wavelengths: 1552.6, 1555.7, 1557.8, 1559.0, and 1561.0 nm (scheme 1); (b) variable AND output under different signal B wavelengths: 1552.9 and 1555.8 nm (scheme 2). Insets are eye diagrams.

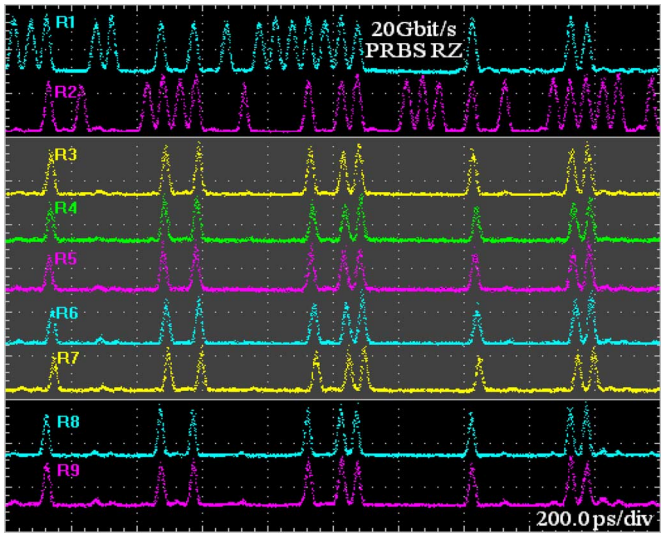

Fig. 3. Waveforms for 20-Gb/s logic AND gate with $2^7 - 1$ PRBS RZ signals. R1: signal A; R2: signal B; R3–R7: tunable AND output corresponding to Fig. 2(a); R8–R9: variable AND output corresponding to Fig. 2(b).

Two operation regimes exist for cSFG/DFG, as shown in Fig. 1(b), depending on whether the SFG occurs between two signals or between one signal and the CW control. For scheme 1, two signals $(\lambda_{SA}, \lambda_{SB})$ generate a sum-frequency (SF) wave through SFG. Meanwhile, the SF wave interacts with the CW control (λ_C) by DFG to yield a converted wave at $1/\lambda_i = 1/\lambda_{SA} + 1/\lambda_{SB} - 1/\lambda_C$. Note that the new generated wave is obtained only when all the three optical waves are present, resulting in the logic AND operation for two data signals. It is worth noting that the AND output can be easily tuned simply by changing the CW control wavelength for fixed data signals. For scheme 2 with SFG occurring between signal A and CW control, the logic AND function can also be performed with the AND output generated at $1/\lambda_i = 1/\lambda_{SA} + 1/\lambda_C - 1/\lambda_{SB}$; thus, variable signal B produces a changeable AND output.

III. Experimental Results

Fig. 2 depicts optical spectra for the 20-Gb/s logic AND gate. For scheme 1 as shown in Fig. 2(a), signals A and B are set at 1549.4 and 1538.3 nm to meet the SFG QPM condition. The generated AND output can be tuned from 1535.3 to 1527.1 nm as the CW control is changed from 1552.6 to 1561.0 nm. For scheme 2 as shown in Fig. 2(b), signal B and CW control wavelengths are exchanged. As a result, the AND output wavelength is determined by signal B wavelength. The AND output at 1535.0 and 1532.1 nm can be obtained when signal B is tuned at 1552.9 and 1555.8 nm.

According to current laboratory conditions, Fig. 3 displays the measured temporal waveforms for the 20-Gb/s logic AND gate by employing $2^7 - 1$ PRBS RZ signals. R1 and R2 represent sample 40-bit sequences of signals A and B, respectively. R3–R7 plot the AND results for scheme 1 shown in Fig. 2(a) with CW control tuned at 1552.6, 1555.7, 1557.8, 1559.0, and 1561.0 nm, respectively. No obvious changes of AND results are found during the tuning process, which implies the successful implementation of tunable logic AND gate. R8 and R9 present the AND results for scheme 2 shown in Fig. 2(b) with signal B set at 1552.9 and 1555.8 nm, respectively. The obtained results shown in Figs. 2 and 3 verify that both two schemes of 20-Gb/s logic AND gate can be successfully implemented.

IV. Numerical Simulations

We further perform simulations of the logic AND gate at 40, 80, and 160 Gb/s, respectively, using the well-known coupled-mode equations describing the cSFG/DFG processes [5], [7]. The waveguide propagation losses of 0.35 dB/cm in the 1.5-μm band and 0.70 dB/cm in the 0.77-μm band are taken into consideration. Other parameters of PPLN are the same as those in [5] and [7]. Two signals A and B are considered as 2^7-1 PRBS RZ data streams with hyperbolic-secant pulse type, 1/3 duty cycle, and 20-dB extinction ratio (ER). The peak powers of two signals and the CW control power are assumed to be 200 mW.

Fig. 4 shows simulation results for ultrahigh-speed logic AND gate. $\lambda_{SA} = 1549.4$ nm, $\lambda_{SB} = 1538.3$ nm, $\lambda_C = 1552.6$ nm for scheme 1, $\lambda_{SA} = 1549.4$ nm, $\lambda_{SB} = 1552.6$ nm, $\lambda_C = 1538.3$ nm for scheme 2 are assumed. Fig. 4(a)–(d) depict waveforms for sample 40-bit sequences of logic AND gate at 40 Gb/s. The AND results for two schemes shown in Fig. 4(c) and (d), the corresponding nice eye opening and high value of the Q-factor and ER shown in Fig. 4(f) and (g) indicate that the proposed cSFG/DFG-based logic AND gate can potentially be operated at 40 Gb/s. The performance degradation of the AND output could be explained by the temporal walk-off effect due to group velocity mismatching (~3 ps/cm) between sum-frequency wave in the 0.77-μm band and signals in the 1.5-μm band [2]. Fig. 4(h)–(j) and (k)–(m) further illustrate the eye diagrams for 80- and 160-Gb/s cSFG/DFG-based logic AND gates, respectively. The length of PPLN is set at 30 mm for 80 Gb/s and 20 mm for 160 Gb/s to avoid the crosstalk between adjacent data bits caused by the walk-off effect. It can be concluded from Fig. 4 that the proposed schemes could be applied to ultrahigh-speed applications. Remarkably, for 160-Gb/s data

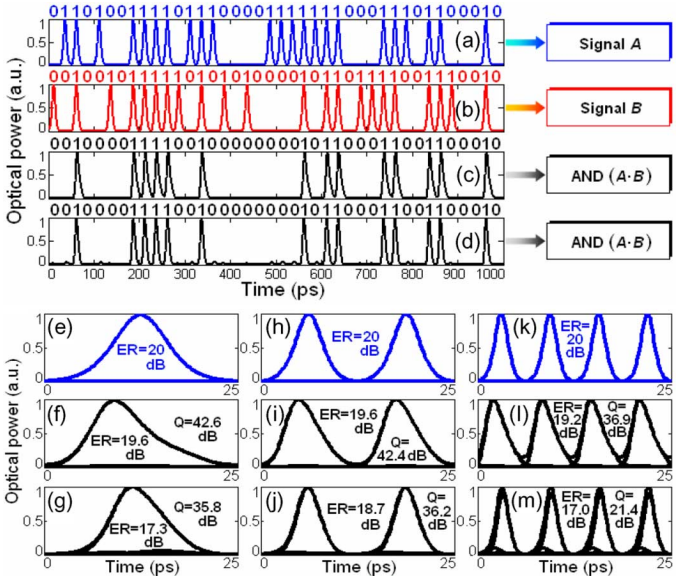

Fig. 4. Waveforms and eye diagrams for ultrahigh-speed logic AND gate; (a)–(g) 40 Gb/s; (h)–(j) 80 Gb/s; (k)–(m) 160 Gb/s; (a)–(d) waveforms; (e)–(m) eye diagrams; (c), (f), (i), (l) scheme 1; (d), (g), (j), (m) scheme 2; (a) signal A; (b) signal B; (e), (h), (k) signal A or B; (c), (d), (f), (g), (i), (j), (l), (m) AND output.

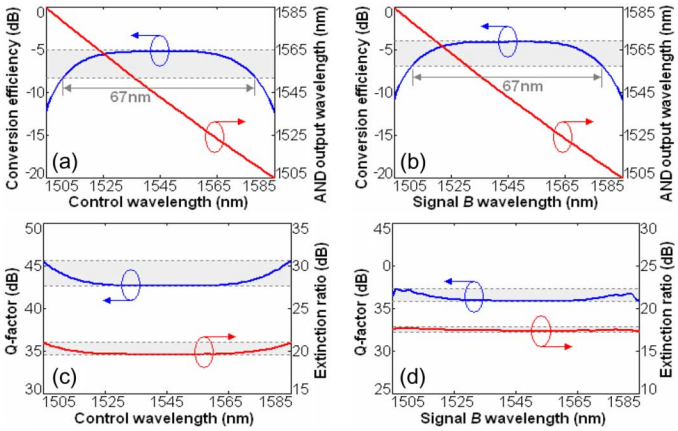

Fig. 5. Tunable performance for 40-Gb/s logic AND gate; (a), (c) scheme 1; (b), (d) scheme 2.

signal with broadband spectrum, as PPLN has the limitation of phase-matching bandwidth to use SFG, the spectrum of output AND is changed, which, however, can potentially be reshaped by reported spectral filtering techniques [4].

Fig. 5 shows the tunable performance for the 40-Gb/s logic AND gate. The length of PPLN is assumed to be 50 mm. The conversion efficiency is defined as the peak power ratio of the AND output to the input signal. As shown in Fig. 5(a) and (b), it is found that the 3-dB conversion bandwidth for both schemes is about 67 nm. Note that the AND output wavelength changes linearly with the control wavelength for scheme 1 and also has a linear relationship with signal B wavelength for scheme 2. As shown in Fig. 5(c) and (d), during the tuning process within the 3-dB conversion bandwidth, it can be clearly seen that the Q-factor and ER changes slightly for both schemes. The wide tuning ranges shown in Fig. 5 imply the flexible logic AND operation with the proposed schemes.

With future improvement, for scheme 1, it is possible to generate tunable multiple AND outputs through the use of changeable multiple CW control waves, which corresponds to tunable multicasting operation. For scheme 2, multiple different AND outputs can be obtained by employing multiple B signals with different data patterns. Also, a three-input high-speed logic AND gate can be performed by replacing the CW control with the third input data signal [11]. In addition, it is expected that the proposed schemes could also be functioned as two- or three-input logic XOR gates when employing RZ differential phase-shift keying input data signals.

V. Conclusion

We have proposed and demonstrated an all-optical tunable logic AND gate at 20 Gb/s based on cSFG/DFG in a PPLN waveguide. It is also possible to perform 40-, 80-, and 160-Gb/s ultrahigh-speed logic AND operations. The theoretical results imply that the AND output can be tuned widely with slight Q-factor and ER fluctuation.

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